IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Christian S. Rode
Appl. No.	:	09 / 287,478
Filed	:	April 6, 1999
Provisional Appl. Filed	:	60 / 080,905, 4/06/98
Title:	:	Apparatus For Evaluating And Demonstrating Electronic Circuits And Components
Grp./A.U.	:	2128
Examiner	:	Thai Phan
Docket No.	:	RCI001v1

Honorable Commissioner for Patents

Washington, D.C. 20231

SUPPLEMENTAL DECLARATION per 37 CFR 1.132

Declaration traversing objection or rejection
(Appendix E2)

As an applicant in the above-identified application, I declare as follows:
1. I am the sole inventor of the subject matter of the above identified application.
2. I have reviewed and understand the contents of the specification and claims, as originally filed, and as amended by the amendment(s) dated
3/25/2002 (as revised 6/13/2002),1/9/2003, 8/28/2003 (as revised 9/29/2003), 5/14/2004, 12/16/2004, and 9/22/2005
3. I believe that I am the original and first inventor or inventors of the subject matter which is claimed and for which a patent is sought.
4. I acknowledge the duty to disclose information which is material to the examination of the application in accordance with 37 C.F.R. Section 1.56(a), and if this oath accompanies or refers to a continuation-in-part application, I acknowledge the duty to disclose material information as defined in 37 C.F.R. Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

In partial fulfillment of Section 1.56(a) please consider the following evidence originally submitted as an Information Disclosure Statement but lacking a statement that this material was discovered within the prior 3 months (in response to Examiner's citation of Xilinx prior art) and so not considered by the Examiner.

PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

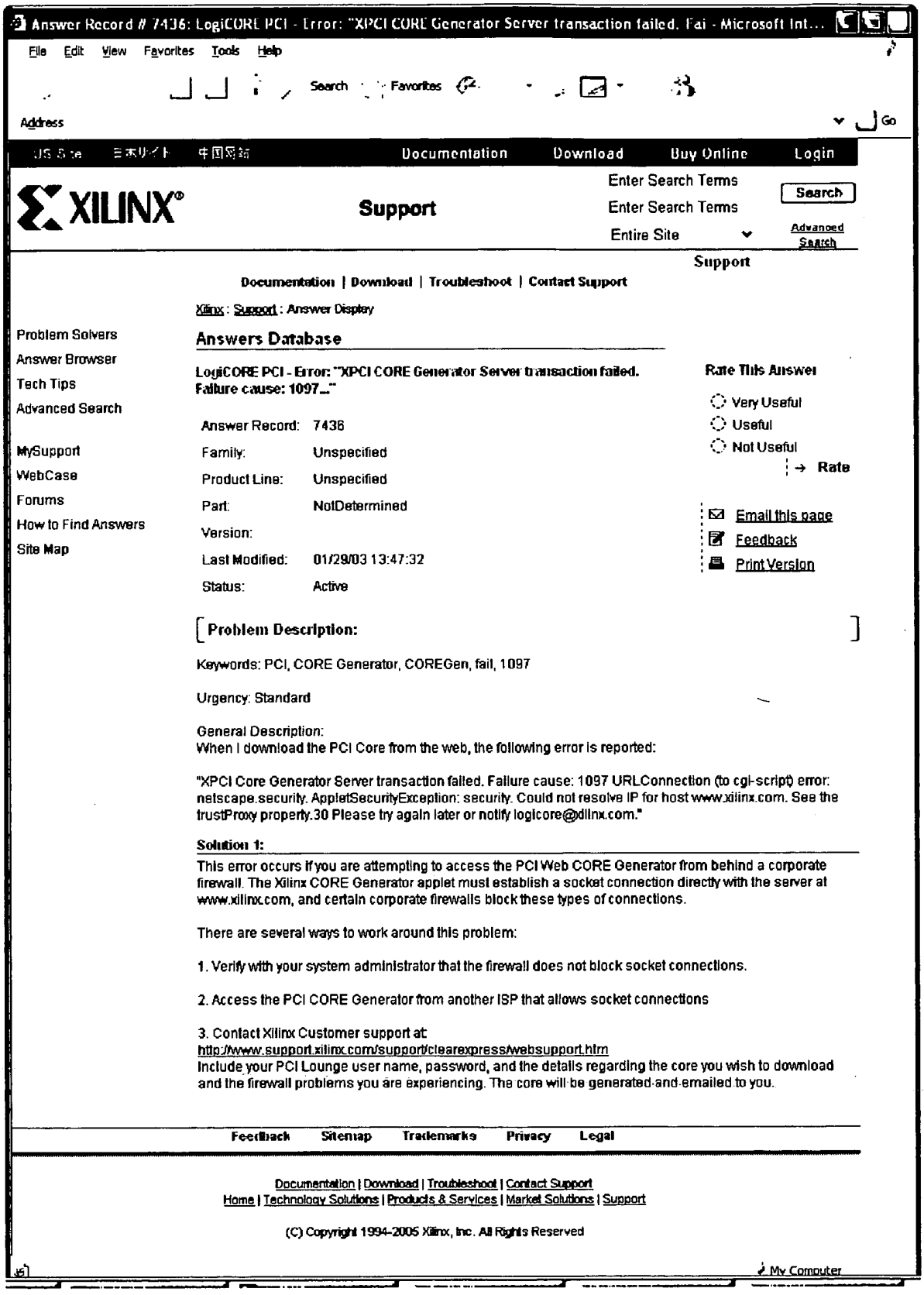
Complete if Known	
Application Number	09/287,478
Filing Date	04/06/1999
First Named Inventor	Christian S. Rode
Art Unit	2128
Examiner Name	Phan, Thai Q.
Attorney Docket Number	RCI001v1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	Answer Record #7436: LogiCORE PCI - Error: "XPCI CORE Generator Server transaction failed. Failure cause: 1097...". Xilinx 2005 [retrieved on October 19, 2005].	
		(cont'd) Retrieved from the Internet: <URL: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=7436>	
	2	CORE Generator for PCI: The First Web-Based Development Tool for FPGA Design. Xilinx, Inc. 1997 [retrieved on October 19, 2005].	
		(cont'd) Retrieved from the Internet: <URL: http://www.xilinx.com/xcell/xl25/xl25_14.pdf>	
	3	CORE Generator Questions & Answers. Xilinx, Inc. 1997 [retrieved on October 19, 2005]. (cont'd)	
		Retrieved from the Internet: <URL: http://www.xilinx.com/products/logicore/pci/cg_qa.htm>	
	4	Email from Mark Noble, Xilinx Technical Support. Xilinx, Inc. Oct 19, 2005	
	5	"Why Choose a Monolithic Instrumentation Amplifier". EDTN / Rode Consutling, 1999. [retrieved on October 19, 2005] Note Xilinx sponsorship.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.


Answer Record # 7436: LogiCORE PCI - Error: "XPCI CORE Generator Server transaction failed. Fai - Microsoft Int...
File Edit View Favorites Tools Help
Search Favorites
Address
Go
Documentation Download Buy Online Login
XILINX®
Support
Enter Search Terms
Enter Search Terms
Search
Entire Site
Advanced Search
Support
Documentation | Download | Troubleshoot | Contact Support
Xilinx : Support : Answer Display
Problem Solvers
Answer Browser
Tech Tips
Advanced Search
MySupport
WebCase
Forums
How to Find Answers
Site Map
Answers Database
LogiCORE PCI - Error: "XPCI CORE Generator Server transaction failed. Failure cause: 1097..."
Answer Record: 7436
Family: Unspecified
Product Line: Unspecified
Part: NotDetermined
Version:
Last Modified: 01/29/03 13:47:32
Status: Active
Rate This Answer
Very Useful
Useful
Not Useful
Rate
Email this page
Feedback
Print Version
Problem Description:
Keywords: PCI, CORE Generator, COREGen, fail, 1097
Urgency: Standard
General Description:
When I download the PCI Core from the web, the following error is reported:
"XPCI Core Generator Server transaction failed. Failure cause: 1097 URLConnection (to cgi-script) error: netscape.security. AppletSecurityException: security. Could not resolve IP for host www.xilinx.com. See the trustProxy property.30 Please try again later or notify logicore@xilinx.com."
Solution 1:
This error occurs if you are attempting to access the PCI Web CORE Generator from behind a corporate firewall. The Xilinx CORE Generator applet must establish a socket connection directly with the server at www.xilinx.com, and certain corporate firewalls block these types of connections.
There are several ways to work around this problem:
1. Verify with your system administrator that the firewall does not block socket connections.
2. Access the PCI CORE Generator from another ISP that allows socket connections
3. Contact Xilinx Customer support at:
http://www.support.xilinx.com/support/clearexpress/websupport.htm
Include your PCI Lounge user name, password, and the details regarding the core you wish to download and the firewall problems you are experiencing. The core will be generated and emailed to you.
Feedback Sitemap Trademarks Privacy Legal
Documentation | Download | Troubleshoot | Contact Support
Home | Technology Solutions | Products & Services | Market Solutions | Support
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Citation 4.1

CORE Generator for PCI: *The First Web-Based Development Tool for FPGA Design*

This spring, Xilinx introduced an innovative, web-based tool that radically simplifies the use of cores for FPGA design. The new, on-line CORE Generator tool facilitates core usage by enabling designers to instantly access, customize, and download core designs using WebLINX (www.xilinx.com).

It features an intuitive graphical interface, thereby shortening the learning curve for logic designers. Initially designed to support users of the LogiCORE PCI module, the CORE Generator will be extended to support other Xilinx LogiCORE and third-party AllianceCORE products later this year.

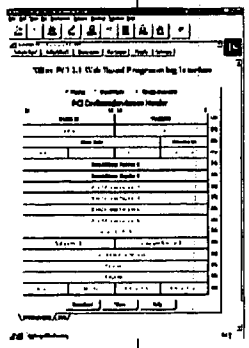


Figure 1: *CORE Generator tool for PCI, main menu*

The CORE Generator tool for PCI introduces a new methodology for acquiring and using cores with FPGAs. Since the tool executes on the web, LogiCORE PCI users always have access to the latest versions of the cores (as well as the latest product information). "Customized" cores are created by the CORE Generator based on user-defined parameters, allowing designers to easily create and download their unique versions of the core netlist, regardless of the design tools and methodologies used for design entry and simulation.

Using CORE Generator

To create a PCI core netlist using the CORE Generator, designers enter their system's parameters by using the program's graphical user interface (GUI). The GUI mirrors the already-familiar PCI Specification Standard table. For example, the GUI includes a copy of the configuration space header from the PCI specification (**Figure 1**); the user simply enters the parameters by selecting the appropriate values in pre-defined menus. The GUI prevents designers from entering invalid parameters. On-line help is available, as well as application notes describing the complete design flow from core configuration to implementation.

The CORE Generator allows the designer to integrate the LogiCORE PCI module using any chosen tool environment, including VHDL, Verilog, or schematic-based design. (Previously, Viewlogic schematic entry tools were required to modify and customize the design.) The CORE Generator creates all the files needed to integrate the PCI core within the FPGA design and verify the results, including:

1) a netlist with constraints that ensure that timing is met without any manual tuning,
2) a "wrapper" used to instantiate the core in a VHDL, Verilog or schematic-based design,
3) a VHDL/Verilog simulation model for functional verification.

These files are then downloaded over the web to the designer's development platform.

The PCI cores created by the CORE Generator are "firm" cores, with relative placement and timing constraints embedded in the netlist to ensure that the performance of the implemented design meets the requirements of the PCI specification. Thus, PCI timing can be met without any manual tuning of the core, and, as a result, engineering resources can be focused on the system-level design, potentially saving months of development time.

Figure 2 compares typical development times and costs for designing a PCI interface from scratch using a generic, synthesizable core and using a proven LogiCORE PCI core.

Visit the VIP Lounge

To access the tool, use a Java-enabled web browser such as Netscape 3.0 or Microsoft Explorer 3.0 to visit WebLINX (www.xilinx.com). The CORE Generator is part of the new "LogiCORE VIP lounge" site that holds useful

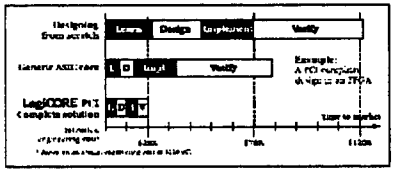
(Continued on page 22)

CORE Generator

(Continued from page 14)

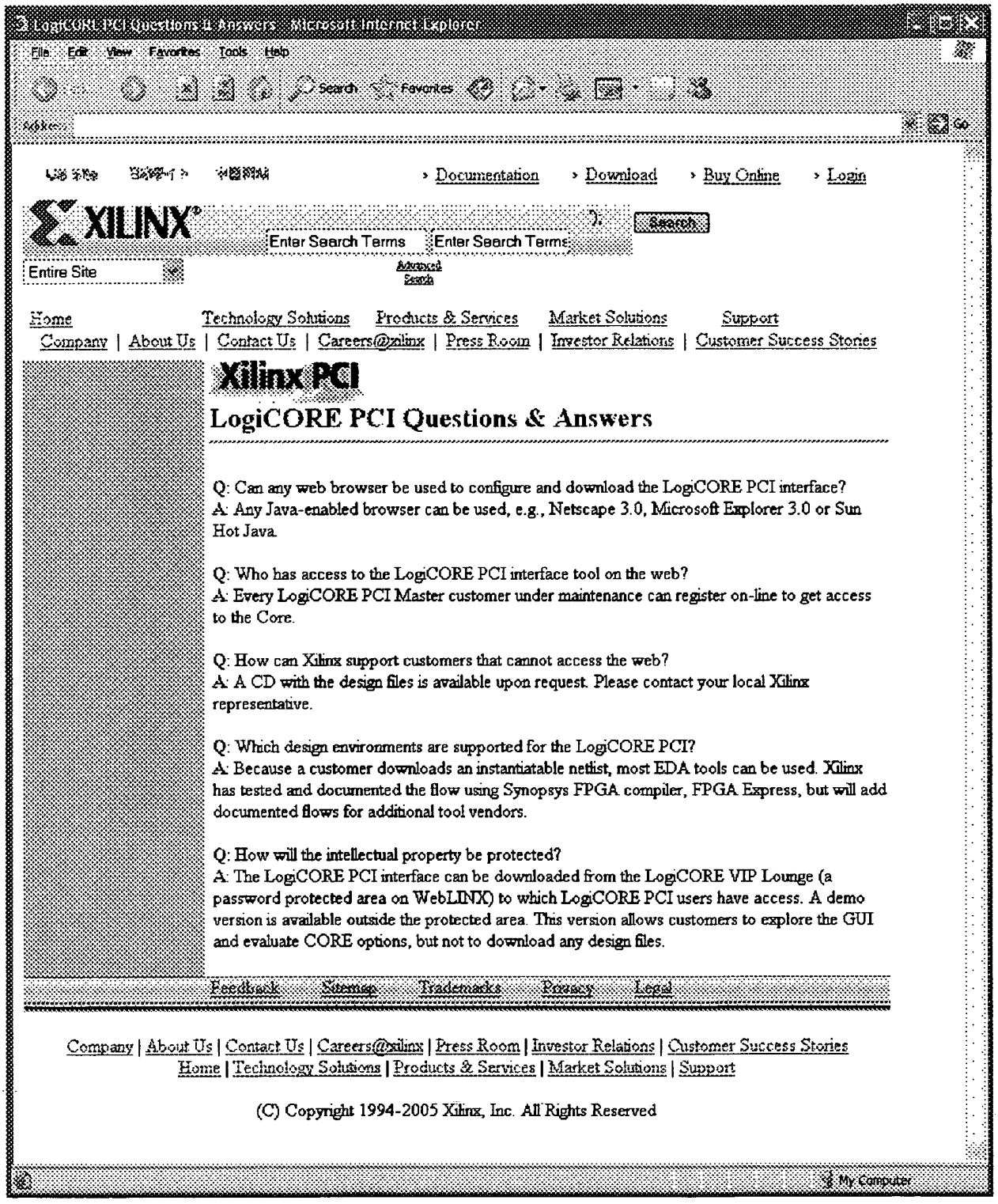
Information and design files for registered LogiCORE product owners; all users with a valid maintenance agreement can log onto the new LogiCORE lounges and register for access to the CORE Generator. The CORE Generator tool is password protected so that only LogiCORE PCI owners have access to the core.

Figure 2: *Proven LogiCORE PCI core cut development time*



For now, even WebLINX visitors without a valid maintenance agreement can access a *demonstration* version of the PCI CORE Generator, allowing the evaluation of the GUI and an examination of the various options available for the PCI interface core. In the future, all visitors will be allowed to create functional simulation models for LogiCORE PCI designs, allowing users to create and download the model, instantiate it into a custom design, and perform complete system functional verification, all prior to purchasing the core.

Further information, including the demonstration version of the CORE Generator, can be found at www.xilinx.com/products/logicore/logicore.htm.◆


LogiCORE PCI Questions & Answers - Microsoft Internet Explorer
File Edit View Favorites Tools Help
Search Favorites
Documentation
Download
Buy Online
Login
XILINX
Enter Search Terms
Search
Entire Site
Advanced Search
Home
Technology Solutions
Products & Services
Market Solutions
Support
Company | About Us | Contact Us | Careers@xilinx | Press Room | Investor Relations | Customer Success Stories
Xilinx PCI
LogiCORE PCI Questions & Answers
Q: Can any web browser be used to configure and download the LogiCORE PCI interface?
A: Any Java-enabled browser can be used, e.g., Netscape 3.0, Microsoft Explorer 3.0 or Sun Hot Java.
Q: Who has access to the LogiCORE PCI interface tool on the web?
A: Every LogiCORE PCI Master customer under maintenance can register on-line to get access to the Core.
Q: How can Xilinx support customers that cannot access the web?
A: A CD with the design files is available upon request. Please contact your local Xilinx representative.
Q: Which design environments are supported for the LogiCORE PCI?
A: Because a customer downloads an instantiatable netlist, most EDA tools can be used. Xilinx has tested and documented the flow using Synopsys FPGA compiler, FPGA Express, but will add documented flows for additional tool vendors.
Q: How will the intellectual property be protected?
A: The LogiCORE PCI interface can be downloaded from the LogiCORE VIP Lounge (a password protected area on WebLINX) to which LogiCORE PCI users have access. A demo version is available outside the protected area. This version allows customers to explore the GUI and evaluate CORE options, but not to download any design files.
Feedback
Sitemap
Trademarks
Privacy
Legal
Company | About Us | Contact Us | Careers@xilinx | Press Room | Investor Relations | Customer Success Stories
Home | Technology Solutions | Products & Services | Market Solutions | Support
(C) Copyright 1994-2005 Xilinx, Inc. All Rights Reserved
My Computer

Citation 4.3

Reply-to: [redacted]

FROM: Mark Noble

******* The following is an email from Xilinx Technical Support.
******* Please do not reply to this email.
******* To reply, send email to the address mark.noble@xilinx.com
******* and reference the case number shown below.

CASE_ID_NUM: 604367

Dear Chris,

With regards to your case:-
CASE #604367

RE: PCI core

The PCI core is still available on the PCI web site, and is provided in a ZIP file only, and their is no WEB CONFIGURATION tool for the PCI core, other than the UCF Generator.

The reason for this is that the PCI core is now included with in the COREGEN tool, as of ISE 7.1i SP2 with IP UPDATE 2. Coregen is capable of providing the PCI core, as well as being able to configure the core with out all the problems that the WEB CONFIGURATION tool had.

The PCI core in coregen is controled by means of a license file which can be obtained form the PCI lounge once the core is purchased. If you have not purchased teh core then you can still generate teh PCI core but will only be able to get the simulation models. If you requier a hardware time out evaluation version of the core, then you will need to reqest a license file for this.

Full information on how to generate an evaluation version of the PCI core can be found at the following web link:-

[redacted]

Best Regards

Mark Noble
Tech Lead
Xilinx Technical Support

/ /\/ For all new technical support issues not in reference to the above
\ \ case, please contact the appropriate support office below. Also
/ / please visit our WEB site at http://support.xilinx.com for the latest
_\/\ Xilinx documentation and application information.
(http://support.xilinx.co.jp for Japanese)

For Customer Education information, please visit
[redacted]

For Technical Support contact information, please visit
[redacted]

Citation 4.4

Why choose a monolithic instrumentation amplifier?
Sponsored by XILINX
Copyright (C) 1998 Bede Consulting, Inc. All rights reserved.

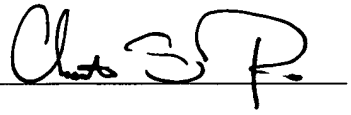
Citation 4.5

This material was not found as part of a general search, but in specific response to examiner's citation of Lawman 6,324,672 (assigned to Xilinx), and therefore more directly connected to Examiner's objections and the content of Applicant's response. To summarize an earlier office action response:

1) Citation 4.1 demonstrates the inability of the Xilinx LogiCORE PCI tool to work through firewalls, which is not a limitation of the present invention;
2) Citation 4.3 demonstrates a requirement for registration by users, which is not a limitation of the present invention;
3) Citation 4.4 suggests a lack of commercial success of the LogiCORE, as it was later withdrawn as a web tool;
4) Citation 4.5 demonstrates that Xilinx was a sponsor of ChipCenter's deployment of the present invention (Articles with embedded interactive simulations); Applicant holds therefore that the citation of Xilinx is in fact an excellent argument in *favor* of nonobviousness since Xilinx effectively licensed the technology of the present invention in preference to using their own.

Applicant had to this point considered the IDS as a neutral mechanism for disclosure of art both prior art and other materials, where 37 CFR 1.132 may have been more appropriate for the latter. In this vein, Applicant would like to point out that the IDS of 1/15/2005 (filed in conjunction with RCE) includes material that *postdates* reduction to practice so as to emphasize the non-obviousness of the present invention at the time of its conception and/or reduction to practice.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Signature of Inventor 

Printed Name of Inventor CHRISTIAN S. RODE

Date 1/19/2007